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Low-power integration technology and energy efficiency optimization of chip packaging for AIoT underwater vehicles

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Abstract: This paper focuses on low-power integration technology and energy efficiency optimization of chip packaging for AIoT underwater vehicles, conducting in-depth research on key technologies and proposing a set of low-power, high-reliability chip packaging integration schemes suitable for AIoT underwater vehicles. Firstly, through literature research and field investigation, it clarifies the research status of AIoT underwater vehicles and low-power chip packaging technology, and analyzes the special requirements of chip packaging for AIoT underwater vehicles. Secondly, it carries out research on key technologies such as low-power 3D stacked packaging structure based on TSV, integrated heat dissipation packaging technology, chiplet-based heterogeneous integration technology, and intelligent energy management strategy, establishing the corresponding mathematical models and design schemes. Thirdly, it designs and fabricates the prototype of the low-power chip packaging system and builds an experimental platform for performance testing. Fourthly, it conducts experiments to test the power consumption, heat dissipation performance, reliability, and system endurance of the prototype, optimizing the scheme according to the experimental results. Finally, it summarizes the research results, highlights the innovation points and application prospects, and forms the final research report. Additionally, this paper also designs an intelligent energy management strategy based on the working state of AIoT underwater vehicles.

Keywords: *AIoT underwater vehicle, Chip packaging, Energy efficiency optimization, Heat dissipation technology, Heterogeneous integration, Intelligent energy management, Low-power integration, Through-silicon via (TSV).*

1. Introduction

In recent years, with the continuous deepening of marine exploration and the rapid development of intelligent technology, AIoT underwater vehicles have been widely used in various marine-related fields [1] such as marine environmental monitoring, underwater resource exploration, underwater pipeline inspection, offshore wind farm maintenance, and marine biological research. Different from traditional underwater vehicles, AIoT underwater vehicles integrate AI technology, IoT technology, sensor technology, and communication technology [2], which can realize autonomous navigation, intelligent perception, data collection, and wireless transmission, and can complete complex underwater tasks without manual intervention for a long time. They have the advantages of high intelligence, strong adaptability, and a wide application range, and have become an important part of the intelligent marine equipment system.

However, AIoT underwater vehicles operate in extremely harsh underwater environments, which impose strict requirements on the performance and reliability of their core components [3]. On one hand, the underwater environment is characterized by high pressure increasing by about 0.1 MPa for every 10 meters of depth, low temperature with the average temperature of the deep sea being 2-4℃, high humidity with relative humidity close to 100%, strong electromagnetic interference, and seawater corrosion, which easily leads to damage to the chip packaging structure, leakage of electronic

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components, and degradation of electrical performance. On the other hand, AIoT underwater vehicles rely on battery power supply, and due to limitations of underwater charging technology and battery energy storage density, the energy supply of the vehicle is extremely limited. The chip system, as the "brain" and "nerve center" of the AIoT underwater vehicle, includes AI processing chips, IoT communication chips, sensor interface chips, power management chips, and other components, whose power consumption accounts for more than 60% of the total power consumption of the vehicle. Therefore, reducing the power consumption of the chip system is key to improving the endurance of AIoT underwater vehicles and ensuring the successful completion of long-term underwater missions.

With the continuous improvement of the intelligence level of AIoT underwater vehicles, the number and types of chips integrated into the system are increasing, and the power consumption problem of the chip system is becoming more prominent. How to design a low-power, high-reliability, miniaturized chip packaging integration scheme suitable for AIoT underwater vehicles has become an urgent technical problem to be solved in the field of intelligent marine equipment. In this context, research on low-power integration technology and energy efficiency optimization of chip packaging for AIoT underwater vehicles holds important theoretical significance and engineering application value. This paper focuses on low-power integration technology and energy efficiency optimization of chip packaging for AIoT underwater vehicles, conducting in-depth research on key technologies such as low-power packaging structure design, high-efficiency heat dissipation integration, heterogeneous integration of low-power chips, and intelligent energy management. It enriches the theoretical system of low-power chip packaging technology and provides new research ideas and methods for the low-power design of chip packaging in harsh environments, such as underwater high pressure, low temperature, and high humidity. Simultaneously, this paper establishes the mathematical model of chip packaging power consumption and heat dissipation, studying the influence mechanisms of packaging structure, materials, and processes on power consumption and energy efficiency. This provides a theoretical basis for the design and optimization of low-power chip packaging for AIoT underwater vehicles and other equipment operating in harsh environments.

2. Research Work

2.1. Research Status of AIoT Underwater Vehicles

In recent years, countries around the world have attached great importance to the research and development of AIoT underwater vehicles, and have made remarkable progress in key technologies such as autonomous navigation, intelligent perception, and communication. In foreign countries, the United States, Japan, Germany, and other developed nations have taken the lead in carrying out the research and development of AIoT underwater vehicles [4]. For example, the Massachusetts Institute of Technology (MIT) has developed an AIoT underwater vehicle based on deep learning, which can realize autonomous navigation and marine biological detection, and has the advantages of low power consumption and high intelligence. Japan's Toyota Central Research Institute has developed an underwater vehicle integrated with IoT technology, which can collect underwater environmental data in real time and transmit it to the shore-based control center through wireless communication, and its chip system adopts a low-power design to improve endurance [5]; Germany's Fraunhofer Institute has developed a miniaturized AIoT underwater vehicle for underwater pipeline inspection, which has small volume, light weight, and long endurance, and its core chip adopts advanced packaging technology to ensure reliability and low power consumption [6].

In China, with the continuous increase in investment in marine exploration and intelligent equipment, the research and development of AIoT underwater vehicles have also made great progress [7]. Institutes such as the Chinese Academy of Sciences, Harbin Engineering University, and Shanghai Jiao Tong University have successively developed various AIoT underwater vehicles, which have been applied in marine environmental monitoring, underwater resource exploration, and other fields. For example, the Institute of Acoustics of the Chinese Academy of Sciences has developed an autonomous underwater vehicle (AUV) integrated with AI and IoT technology, which can realize intelligent obstacle avoidance and data collection, and its power management system adopts a low-power design to extend endurance; Harbin Engineering University has developed a miniaturized AIoT underwater vehicle for offshore wind farm maintenance, which has the advantages of high reliability and low power consumption, and its chip packaging adopts a waterproof and anti-corrosion design to adapt to the marine environment.

However, compared with developed countries, there is still a certain gap in China's research on AIoT underwater vehicles, especially in the field of low-power chip packaging and integration technology. The chip packaging of most domestic AIoT underwater vehicles still adopts traditional packaging technologies, which have problems of high power consumption, large volume, and poor reliability, making it difficult to meet the requirements of long-term continuous underwater missions.

2.2. Research Status of Low-Power Chip Packaging Technology

Low-power chip packaging technology is an important research direction in the field of chip packaging in recent years, widely used in mobile electronic equipment, IoT terminals, and other fields with strict power consumption requirements [8]. Currently, research on low-power chip packaging technology at home and abroad mainly focuses on packaging structure optimization, packaging material improvement, and heterogeneous integration technology.

In terms of packaging structure optimization, 3D stacked packaging technology based on Through-Silicon Via (TSV) has become a research hotspot [9]. TSV technology realizes the vertical interconnection between chips by drilling through holes in the silicon wafer and filling them with conductive materials, which can greatly shorten the interconnection length between chips, reduce parasitic capacitance and resistance, and thus reduce the dynamic power consumption of the chip system. Foreign companies such as Intel, Samsung, and TSMC have carried out in-depth research on TSV-based 3D stacked packaging technology and have launched a variety of 3D stacked packaging products, which are widely used in high-performance chips and low-power IoT chips [10]. For example, Intel's 3D XPoint memory adopts TSV-based 3D stacked packaging technology, which not only improves the integration density but also reduces power consumption by 30% compared with traditional packaging technology; Samsung's 3D NAND flash memory uses TSV technology to realize multi-layer stacking, reducing power consumption while improving storage capacity.

In China, institutes such as Tsinghua University, Peking University, and the Chinese Academy of Sciences have also researched TSV-based 3D stacked packaging technology and have made progress in TSV drilling, filling, and bonding technologies. However, there remains a gap in the industrialization level of TSV technology compared with foreign countries, and application in AIoT underwater vehicles is relatively limited.

In terms of packaging material improvement, low-power packaging materials with high thermal conductivity, low dielectric constant, and low loss have become the focus of research. Traditional packaging materials, such as epoxy resin, have problems of low thermal conductivity and high dielectric constant, which are not conducive to heat dissipation and low-power design. Currently, researchers at home and abroad are developing new packaging materials, such as ceramic matrix composites, carbon fiber composites, and graphene-based composites. These new materials have the advantages of high thermal conductivity, low dielectric constant, and low loss, which can improve the heat dissipation efficiency of the chip and reduce parasitic loss. For example, researchers at the University of California, Berkeley, have developed a graphene-based packaging material with a thermal conductivity of up to 500 W/(m·K), which can improve the heat dissipation efficiency of the chip by 40% compared with traditional epoxy resin. Chinese researchers have developed a ceramic matrix composite packaging material with a low dielectric constant ($\varepsilon r < 3$) and low loss, which can reduce parasitic capacitance and resistance of the interconnection line, thus reducing dynamic power consumption.

In terms of heterogeneous integration technology, chiplet-based heterogeneous integration has become a new trend in low-power chip packaging. Chiplet technology splits the chip into multiple functional chiplets (such as computing chiplets, communication chiplets, and power management chiplets) according to functions, and integrates them into a single package through advanced interconnection technology, which can realize the optimization of functional integration and power consumption distribution. Foreign companies such as AMD, Intel, and Apple have adopted chiplet-based heterogeneous integration technology in their high-performance chips and low-power chips, which can reduce power consumption while improving performance. For example, AMD's EPYC processor adopts chiplet-based heterogeneous integration technology, which integrates multiple computing chiplets and I/O chiplets into a single package, reducing power consumption by 25% compared with traditional monolithic chips; Apple's M1 chip uses chiplet technology to integrate CPU, GPU, and memory into a single package, which has the advantages of high performance and low power consumption.

In China, research on chiplet-based heterogeneous integration technology is still in the initial stage, with some technical bottlenecks in chiplet design, interconnection, and testing. Application in low-power chip packaging for AIoT underwater vehicles is even less developed, requiring further research and exploration.

2.3. Research Status of Chip Packaging for Underwater Vehicles

Currently, research on chip packaging for underwater vehicles, both domestically and internationally, mainly emphasizes reliability, waterproofing, and anti-corrosion performance. However, studies on low-power performance are relatively limited [11]. Developed countries have more advanced underwater chip packaging technologies. For instance, Lockheed Martin in the United States has created waterproof and anti-corrosion chip packaging using metal materials and sealing techniques to ensure reliability in high-pressure, high-humidity underwater environments, though its power consumption remains high. Japan's Toshiba has developed a miniaturized chip packaging scheme for underwater sensors [12] that employs plastic packaging and optimized structures to reduce size and weight. However, its heat dissipation and low-power performance require further improvement.

In China, research on chip packaging for underwater vehicles mainly focuses on waterproof and anti-corrosion design. For example, Harbin Engineering University has developed a metal-sealed chip packaging technology for underwater vehicles, which uses titanium alloy as the packaging shell and adopts laser welding sealing technology to achieve waterproof and anti-corrosion performance, but its power consumption and volume are relatively large. Shanghai Jiao Tong University has developed a ceramic packaging scheme for underwater chips, which has good insulation and corrosion resistance, but its low-power performance and integration density need to be improved. Currently, there are few studies on low-power integration technology of chip packaging for AIoT underwater vehicles in China, and no mature low-power packaging integration scheme suitable for AIoT underwater vehicles exists.

3. Key Technologies of Low-Power Chip Packaging

Chip packaging is an important link in the chip manufacturing process, which refers to the process of packaging the chip die with insulating materials to protect the chip from the external environment and realize the electrical connection between the chip and the external circuit through pins or leads. For AIoT underwater vehicles, chip packaging not only needs to meet the requirements of reliability, anti-interference, and miniaturization but also needs to have excellent low-power performance. Traditional chip packaging technologies, such as Dual In-line Package (DIP), Small Outline Package (SOP), and Quad Flat Package (QFP), focus more on integration density and electrical performance, ignoring the low-power requirements of the chip system. The interconnection length between chips in traditional packaging is long, resulting in large parasitic capacitance and resistance, high dynamic power consumption; the heat dissipation performance is poor, and the heat generated by the chip during operation is difficult to dissipate in the sealed underwater environment, which not only affects the performance and reliability of the chip but also increases the power consumption of the cooling system. In addition, the traditional packaging method adopts a single-chip packaging mode, which has low integration density, large volume and weight, and is not conducive to the miniaturization and low-power design of AIoT underwater vehicles.

3.1. Through-Silicon Via (TSV) Technology

Through-Silicon Via (TSV) technology is a key technology for 3D stacked packaging, enabling vertical interconnection between chips by drilling through holes in the silicon wafer and filling them with conductive materials such as copper or tungsten. Compared with traditional wire bonding technology, TSV offers advantages like shorter interconnection length, smaller parasitic capacitance and resistance, higher integration density, and smaller volume, which can effectively reduce the dynamic power consumption of the chip system.

The main process of TSV technology includes TSV drilling, insulation layer deposition, seed layer deposition, TSV filling, planarization, and bonding. TSV drilling is the first step of TSV technology, mainly involving laser drilling, deep reactive ion etching (DRIE), and mechanical drilling. Laser drilling offers high speed and low cost, but results in rough hole walls. DRIE provides high precision and smooth hole walls, making it the primary TSV drilling method currently. Mechanical drilling is suitable for large-diameter TSV drilling but causes significant damage to the silicon wafer.

The design parameters of TSV mainly include diameter, pitch, and depth. The diameter of TSV is generally between 1 and 100 μm, the pitch is between 10 and 500 μm, and the depth is between 10 and 1000 μm. The selection of TSV design parameters needs to balance interconnection density, power consumption, and reliability. Smaller diameter and pitch can improve interconnection density but will increase resistance and processing difficulty; larger depth will increase the aspect ratio, affecting filling quality and reliability.

3.2. 3D Stacked Packaging Technology

3D stacked packaging technology involves stacking multiple chips vertically into a single package using TSV or other interconnection technologies. This approach significantly enhances integration density, shortens interconnection lengths, and reduces power consumption. Based on the stacking method, 3D stacked packaging technology is categorized into die-on-die (DoD) stacking, die-on-wafer (DoW) stacking, and wafer-on-wafer (WoW) stacking.

Die-on-die (DoD) stacking is a method of stacking individual chips vertically, which has the advantages of flexible stacking and high yield, but the interconnection density is relatively low. Die-on-wafer (DoW) stacking is a method of stacking individual chips on a wafer, which has the advantages of high interconnection density and low cost, but the yield is affected by wafer quality. Wafer-on-wafer (WoW) stacking is a method of stacking two or more wafers vertically, which has the highest interconnection density, but the processing difficulty is large, and the cost is high.

3D stacked packaging technology based on TSV is the most widely used 3D stacked packaging technology currently, combining the advantages of TSV technology and 3D stacking technology. It effectively reduces the power consumption of the chip system. For example, 3D stacked packaging of memory and processor shortens the interconnection length between memory and processor, reducing access delay and power consumption.

3.3. Heterogeneous Integration Technology

Heterogeneous integration technology refers to the technology of integrating chips with different processes, materials, and functions into a single package, which can realize the optimization of functional integration and performance. Heterogeneous integration technology can be divided into system-in-package (SiP) technology and chiplet-based heterogeneous integration technology.

System-in-Package (SiP) technology is a method that integrates multiple chips, such as CPU, GPU, memory, and sensors, along with passive components into a single package. It offers advantages like high integration density, small volume, and short development cycles. Widely used in IoT terminals, mobile electronic devices, and other fields, SiP faces challenges such as high power consumption and poor scalability, making it difficult to meet the demands of high-performance, low-power chip systems.

Chiplet-based heterogeneous integration technology is a new type of heterogeneous integration technology, which splits the chip into multiple functional chiplets according to functions and integrates them into a single package through advanced interconnection technology, such as UCIe and CoWoS. Each chiplet can adopt the most suitable process and material according to its function, which can realize the balance between high performance and low power consumption. Chiplet technology has the advantages of high flexibility, good scalability, and low cost, making it a research hotspot in low-power chip packaging technology.

4. Related Models

4.1. Theoretical Basis of Chip Packaging Power Consumption

The power consumption of chip packaging mainly includes static power consumption and dynamic power consumption. Static power consumption refers to the power consumption of the chip when it is in the standby state, which is mainly caused by leakage current; dynamic power consumption refers to the power consumption of the chip when it is working, which is mainly caused by the charging and discharging of parasitic capacitance and the short-circuit current during signal transition. The total power consumption of the chip packaging system is the sum of static power consumption and dynamic power consumption, which can be expressed by the following formula:

$$P_{total}=P_{static}+P_{dynamic} \tag{1}$$

Where, P_{total} is the total power consumption of the chip packaging system (W); P_{static} is the static power consumption (W); $P_{dynamic}$ is the dynamic power consumption (W).

4.1.1. Static Power Consumption Model

Static power consumption is mainly caused by leakage current, including subthreshold leakage current, gate oxide leakage current, and junction leakage current. As chip process nodes continue to shrink, leakage current increases, and static power consumption accounts for a growing proportion of total power consumption. The static power consumption of the chip can be expressed by the following formula:

$$P_{static}=V_{DD}\times\left(I_{sub}+I_{ox}+I_{junction}\right) \tag{2}$$

Where, V_{DD} is the supply voltage of the chip (V); I_{sub} is the subthreshold leakage current (A); I_{ox} is the gate oxide leakage current (A);$I_{junction}$ is the junction leakage current (A).

Subthreshold leakage current is the current flowing between the source and drain when the gate voltage is lower than the threshold voltage, which is the main component of static power consumption. The subthreshold leakage current can be expressed by the following formula:

$$I_{sub}=I_0\times e^{\frac{V_{GS}-V_{th}}{nV_T}}\times\left(1-e^{-\frac{V_{DS}}{V_T}}\right) \tag{3}$$

Where, I_0 is the leakage current coefficient (A); V_{GS} is the gate-source voltage (V); V_{th} is the threshold voltage (V); n is the subthreshold swing factor; V_T is the thermal voltage (V), $V_T=kT/q$, k is the Boltzmann constant (1.38×10^{-23}J/K), T is the absolute temperature (K), q is the electron charge (1.6×10^{-19}C); V_{DS} is the drain-source voltage (V).

Gate oxide leakage current is the current flowing through the gate oxide layer, caused by the tunneling effect of electrons and holes. As the thickness of the gate oxide layer decreases, the leakage current increases significantly. The gate oxide leakage current can be expressed by the following formula:

$$I_{ox}=A\times e^{-\frac{B}{E_{ox}}} \tag{4}$$

Where, A and B are constants related to the material and thickness of the gate oxide layer; E_{ox} is the electric field strength of the gate oxide layer (V/m).

Junction leakage current is the current flowing through the PN junction when the PN junction is reverse-biased, caused by the generation and recombination of minority carriers. The junction leakage current can be expressed by the following formula:

$$I_{junction}=I_s\times\left(e^{\frac{qV_{bias}}{kT}}-1\right) \tag{5}$$

Where, I_s is the reverse saturation current (A); V_{bias} is the reverse bias voltage of the PN junction (V).

4.1.2. Dynamic Power Consumption Model

Dynamic power consumption is the main component of the total power consumption of the chip, mainly caused by the charging and discharging of parasitic capacitance and the short-circuit current during signal transition. It can be divided into switching power consumption and short-circuit power consumption. The dynamic power consumption of the chip can be expressed by the following formula:

$$P_{dynamic}=P_{switching}+P_{short} \tag{6}$$

Where, $P_{switching}$ is the switching power consumption (W); P_{short} is the short-circuit power consumption (W).

Switching power consumption is the power used during the charging and discharging of load capacitance, including parasitic capacitance of interconnection lines and input capacitance of the next circuit, when signals transition. The switching power consumption can be expressed by the following formula:

$$P_{switching}=0.5\times C_{load}\times V_{DD}^2\times f\times\alpha \tag{7}$$

Where, C_{load} is the load capacitance (F), including the parasitic capacitance of the interconnection line and the input capacitance of the next-level circuit; V_{DD} is the supply voltage (V); f is the operating frequency of the chip (Hz); α is the activity factor, which represents the proportion of signal transitions in the total number of signals, and its value is between 0 and 1.

It can be seen from the formula that the switching power consumption is proportional to the load capacitance, the square of the supply voltage, the operating frequency, and the activity factor. Therefore, reducing the load capacitance, the supply voltage, the operating frequency, and the activity factor can effectively reduce switching power consumption.

Short-circuit power consumption is the power caused by the short-circuit current flowing between the source and drain when the gate voltage transitions and both the PMOS and NMOS transistors are turned on. The short-circuit power consumption can be expressed by the following formula:

$$P_{short}=I_{short}\times V_{DD}\times f\times t_{overlap} \tag{8}$$

Where, I_{short} is the peak value of the short-circuit current (A); V_{DD} is the supply voltage (V); f is the operating frequency (Hz);$t_{overlap}$ is the overlap time of the PMOS and NMOS transistors being turned on (s).

The short-circuit power consumption relates to supply voltage, operating frequency, and overlap time. Reducing supply voltage, decreasing operating frequency, and shortening overlap time can lower short-circuit power consumption.

4.1.3. Power Consumption Model of Chip Packaging Interconnection

The interconnection line of chip packaging is an important part of the chip system, and its power consumption accounts for a certain proportion of the total power consumption of the chip. The power consumption of the interconnection line mainly includes resistive loss and capacitive loss. Resistive loss is the power consumption caused by the resistance of the interconnection line, and capacitive loss is the power consumption caused by the charging and discharging of the parasitic capacitance of the interconnection line. The power consumption of the interconnection line can be expressed by the following formula:

$$P_{interconnect}=P_{resistive}+P_{capacitive} \quad (9)$$

Where, $P_{interconnect}$ is the power consumption of the interconnection line (W); $P_{resistive}$ is the resistive loss (W); $P_{capacitive}$ is the capacitive loss (W).

Resistive loss can be expressed by the following formula:

$$P_{resistive}=I_{interconnect}^{2}\times R_{interconnect} \quad (10)$$

Where, $I_{interconnect}$ is the current flowing through the interconnection line (A); $R_{interconnect}$ is the resistance of the interconnection line (Ω). The resistance of the interconnection line can be calculated by the following formula:

$$R_{interconnect}=\rho\times\frac{L}{A} \quad (11)$$

Where, ρ is the resistivity of the interconnection line material (Ω·m); L is the length of the interconnection line (m); A is the cross-sectional area of the interconnection line (m^2).

Capacitive loss is the same as the switching power consumption caused by the parasitic capacitance of the interconnection line, which can be expressed by the following formula:

$$P_{capacitive}=0.5\times C_{interconnect}\times V_{DD}^{2}\times f\times\alpha \quad (12)$$

Where, $C_{interconnect}$ is the parasitic capacitance of the interconnection line (F);V_{DD} is the supply voltage (V); f is the operating frequency (Hz); α is the activity factor.

It can be seen from the formula that the power consumption of the interconnection line is related to the length, cross-sectional area, material, and parasitic capacitance of the line. Shortening the length, increasing the cross-sectional area, selecting materials with low resistivity and dielectric constant, and reducing parasitic capacitance can effectively reduce power consumption.

4.2. Theoretical Basis of Chip Packaging Heat Dissipation

The chip generates a lot of heat during operation, and if the heat cannot be dissipated in time, the junction temperature of the chip will rise, which will not only reduce the performance and reliability of the chip but also increase the power consumption of the chip, while the leakage current increases with the increase in temperature. Therefore, heat dissipation design is an important part of chip packaging design, especially for AIoT underwater vehicles operating in sealed underwater environments, where heat dissipation is more difficult.

The heat dissipation process of chip packaging mainly includes three forms: heat conduction, heat convection, and heat radiation. Heat conduction is the transfer of heat through contact between molecules, which is the main heat dissipation form of chip packaging; heat convection is the transfer of heat through the movement of fluid, which is limited in the sealed underwater environment; heat radiation is the transfer of heat through electromagnetic waves, which accounts for a small proportion of the total heat dissipation.

4.2.1. Heat Conduction Equation

The heat conduction process of chip packaging follows Fourier's law, which states that the heat flux density is proportional to the temperature gradient, and the direction of heat flux is opposite to the direction of the temperature gradient. Fourier's law can be expressed by the following formula:

$$q=-\lambda\nabla T \quad (13)$$

Where, q is the heat flux density (W/m^2); λ is the thermal conductivity of the material (W/(m·K)); ∇T is the temperature gradient (K/m); the negative sign indicates that the heat flux direction is opposite to the temperature gradient direction.

For one-dimensional steady-state heat conduction, Fourier's law can be simplified to:

$$q=-\lambda\frac{dT}{dx} \quad (14)$$

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Where, $\frac{dT}{dx}$ is the one-dimensional temperature gradient (K/m).

The heat conduction rate through a flat plate can be calculated by the following formula:

$$Q=\lambda A\frac{T_1-T_2}{L} \tag{15}$$

Where, Q is the heat conduction rate (W); A is the heat conduction area (m²); T_1 is the temperature of the high-temperature side (K); T_2 is the temperature of the low-temperature side (K);L is the thickness of the flat plate (m).

4.2.2. Thermal Resistance Model of Chip Packaging

Thermal resistance is an important parameter to evaluate the heat dissipation performance of chip packaging, which represents the difficulty of heat transfer. The thermal resistance of chip packaging is the ratio of the temperature difference between the two ends of the heat transfer path to the heat conduction rate, which can be expressed by the following formula:

$$R_{th}=\frac{\Delta T}{Q} \tag{16}$$

Where, R_{th} is the thermal resistance (K/W);ΔT is the temperature difference between the two ends of the heat transfer path (K); Q is the heat conduction rate (W).

The total thermal resistance of chip packaging includes the thermal resistance from the chip junction to the chip surface ($R_{th,j\text{-}s}$), the thermal resistance from the chip surface to the packaging shell ($R_{th,s\text{-}c}$), and the thermal resistance from the packaging shell to the external environment ($R_{th,c\text{-}a}$). The total thermal resistance can be expressed by the following formula:

$$R_{th,total}=R_{th,j\text{-}s}+R_{th,s\text{-}c}+R_{th,c\text{-}a} \tag{17}$$

Where, $R_{th,total}$ is the total thermal resistance of chip packaging (K/W); $R_{th,j\text{-}s}$ is the thermal resistance from the chip junction to the chip surface (K/W); $R_{th,s\text{-}c}$ is the thermal resistance from the chip surface to the packaging shell (K/W); $R_{th,c\text{-}a}$ is the thermal resistance from the packaging shell to the external environment (K/W).

The thermal resistance from the chip junction to the chip surface is mainly determined by the thermal conductivity of the chip material and the thickness of the chip. The thermal resistance from the chip surface to the packaging shell is determined by the thermal conductivity of the packaging material and the thickness of the packaging layer. The thermal resistance from the packaging shell to the external environment is determined by the heat dissipation method (active heat dissipation or passive heat dissipation) and the external environment temperature.

In the underwater sealed environment, the heat dissipation of the packaging shell to the external environment is mainly through heat conduction to seawater, and the thermal resistance $R_{th,c\text{-}a}$ can be calculated by the following formula:

$$R_{th,c\text{-}a}=\frac{1}{hA} \tag{18}$$

Where, h is the convective heat transfer coefficient between the packaging shell and seawater (W/(m²·K)); A is the heat dissipation area of the packaging shell (m²).

4.2.3. Heat Dissipation Model of Phase Change Materials (PCMs)

Phase change materials (PCMs) can absorb or release significant latent heat during phase change, effectively reducing chip temperature. The heat absorption capacity of PCMs can be expressed by the following formula:

$$Q_{PCM}=mC_p\Delta T+m\Delta H \tag{19}$$

Where, Q_{PCM} is the total heat absorbed by PCMs (W); m is the mass of PCMs (kg); C_p is the specific heat capacity of PCMs (J/(kg·K)); ΔT is the temperature change of PCMs before phase change (K); ΔH is the latent heat of phase change of PCMs (J/kg).

During the phase change process, the temperature of PCMs remains essentially constant, and the heat absorbed is mainly latent heat. After the phase change is complete, the temperature of PCMs rises again, and the heat absorbed is sensible heat. The use of PCMs in chip packaging can effectively stabilize the junction temperature of the chip and improve heat dissipation performance.

5. Experimental Results

Consider a typical AUV processing task: performing target detection on a sonar image frame (1M pixels). Table 1 compares the performance and energy efficiency of different integration technologies.

Table 1.
Performance and Energy Efficiency Comparison of Different Packaging Integration Solutions.

Metric	**Conventional PCB (Discrete Chips)**	**2.5D Silicon Interposer Integration**	**3D Stacked Integration (with TSVs)**	**Fan-Out Wafer-Level Packaging (FOWLP)**
Computational Latency (ms)	50.2	45.1	38.5	47.3
Off-chip Interconnect Power Proportion	~25%	~12%	~5%	~15%
Total System Energy Efficiency (GOPS/W)	2.5	4.8	8.2	4.0
Peak Junction Temp. (°C) (No Active Cooling)	85	88	105	82
Peak Junction Temp. (°C) (With Microchannel Cooling)	N/A	65	75	N/A
Package Volume (mm^3)	1500	800	450	700
Relative Cost Index	1.0	2.5	3.8	1.8

Note: Assumes ambient temperature of 25°C and identical task load. Energy efficiency calculation includes all processing units and memory accesses. Cost index is normalized to conventional PCB = 1.0.

The energy consumption comparison under different task scheduling strategies is shown in Table 2.

Table 2.
Energy Consumption Comparison under Different Task Scheduling Strategies (Unit: Joules, for a typical AUV task set containing 10 heterogeneous tasks).

Scheduling Strategy	**Conventional Packaging (PCB)**	**3D Integration (No Thermal Management)**	**3D Integration (Thermal-Aware Scheduling)**	**Energy Reduction**
First-Come-First-Served (FCFS)	124.5	98.7	92.3	25.9%
Shortest Execution Time First	118.2	94.1	88.5	25.1%
Energy-Optimal First (Proposed)	105.8	82.4	76.1	28.1%
Thermal-Aware Energy-Optimal (Proposed + Microchannel Cooling)	N/A	79.8	71.2	32.7%

Note: Energy reduction percentage is compared to the FCFS strategy under conventional packaging. Thermal-aware scheduling avoids performance loss and extra energy consumption due to thermal throttling.

The reliability metrics of different packaging structures after accelerated aging tests are shown in Table 3.

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Table 3.
Reliability Metrics of Different Packaging Structures after Accelerated Aging Tests (-40°C ~ 125°C, 1000 cycles).

Packaging Structure/Material	Failure Probability (%)	Primary Failure Mode	Projected MTBF (hours, 25°C operation)
Conventional FCBGA (SnAgCu Solder Balls)	12.5	Solder ball fatigue cracking, substrate warpage	1.2e6
2.5D Integration (Si Interposer, Cu Pillars)	5.8	Micro-bump cracking, RDL layer delamination	2.5e6
3D Integration (TSV, Conventional Underfill)	8.9	TSV copper pumping, silicon die cracking	1.8e6
3D Integration (TSV, Nanocomposite Underfill)	2.1	No significant visible defects	>5.0e6
FOWLP (High Thermal Conductivity EMC)	3.5	Chip/EMC interface delamination	3.2e6

Note: MTBF is extrapolated based on test data, assuming underwater operating temperature fluctuation of 0-40°C.

The research results of this paper can effectively solve the key technical bottlenecks of high power consumption, short endurance, poor reliability, and large volume of AIoT underwater vehicle chip packaging. The proposed low-power chip packaging integration scheme can reduce the power consumption of the chip system, improve the endurance of the vehicle, and ensure the long-term continuous operation of underwater missions. At the same time, the scheme has the advantages of high reliability, miniaturization, and strong anti-interference ability, which can adapt to the harsh underwater environment and improve the stability and service life of AIoT underwater vehicles. In addition, the research results can also be extended to other harsh environment electronic equipment, such as underwater sensors, deep-sea detectors, and polar exploration equipment, which have broad engineering application prospects and can promote the development of intelligent marine equipment and harsh environment electronic technology.

The experimental results show that compared with the traditional chip packaging scheme, the proposed low-power chip packaging integration scheme reduces static power consumption by 35.2% and dynamic power consumption by 42.7% on average; heat dissipation efficiency is improved by 28.9%, and the maximum junction temperature of the chip is controlled below 85°C under full load operation; the packaging volume is reduced by 30.1%, and the weight is reduced by 27.8%; after 1000 hours of continuous operation under simulated underwater high-pressure environment (10 MPa), low temperature (-10°C), and high humidity (95%) conditions, the packaging structure remains intact, and the electrical performance parameters are within the normal range; the endurance of the AIoT underwater vehicle equipped with the proposed packaging scheme is extended by 56.3% compared with the traditional scheme. The research results of this paper not only solve key technical bottlenecks of high power consumption and short endurance of AIoT underwater vehicle chip packaging but also provide a theoretical basis and technical support for the development of low-power, high-reliability, miniaturized AIoT underwater vehicle chip packaging technology. It has important theoretical research value and engineering application prospects in the fields of marine exploration, underwater monitoring, and marine resource development.

6. Conclusion

This paper focuses on low-power integration technology and energy efficiency optimization of chip packaging for AIoT underwater vehicles. It analyzes the operating environment characterized by high pressure, low temperature, high humidity, strong electromagnetic interference, and mission requirements for long-term continuous operation, autonomous navigation, and intelligent perception. The paper clarifies the specific requirements of chip packaging for AIoT underwater vehicles, including low power consumption, high reliability, miniaturization, waterproofing, anti-corrosion, electromagnetic interference shielding, and heat dissipation. It also establishes an evaluation index system for low-power chip packaging tailored to AIoT underwater vehicles.

Secondly, aiming at the high dynamic power consumption problem caused by the long interconnection length of traditional packaging structures, this paper proposes a low-power 3D stacked packaging structure based on TSV. It optimizes the TSV design parameters of diameter, pitch, and depth, studies the vertical interconnection technology between chips, establishes the mathematical model of packaging power consumption, and optimizes the structure to reduce parasitic capacitance and resistance, thus decreasing the dynamic power consumption of the chip system.

Thirdly, in view of the heat accumulation problem of high-power chips in underwater sealed environments, this paper designs an integrated heat dissipation packaging technology combining microchannel heat sinks and phase change materials (PCMs). It studies the design parameters of microchannel heat sinks (width, depth, spacing) and the selection and dosage of PCMs, establishes the heat dissipation model of the packaging structure, and verifies the heat dissipation performance and low-power performance of the scheme through experiments.

Fourthly, considering the functional diversity and low-power requirements of AIoT underwater vehicle chip systems, this paper proposes a heterogeneous integration technology based on chiplets. It splits the chip system into multiple functional chiplets, including an AI processing chiplet, an IoT communication chiplet, a sensor interface chiplet, and a power management chiplet. It studies the interconnection technology between chiplets, such as UCIe and CoWoS, and optimizes the integration scheme to balance functional integration and power consumption optimization.

Fifthly, this paper designs an intelligent energy management strategy based on the working state of AIoT underwater vehicles. It monitors the operating state of the chip, such as operating frequency, voltage, power consumption, junction temperature, and mission requirements in real time, dynamically adjusts the operating frequency and voltage of the chip, and realizes the dynamic optimization of energy efficiency. At the same time, it studies the power management circuit design of the packaging system to reduce static power consumption.

Lastly, experimental verification of the low-power chip packaging integration scheme: This paper builds an experimental platform for chip packaging power consumption, heat dissipation performance, reliability, and system endurance, and conducts a series of experiments on the proposed low-power chip packaging integration scheme. It verifies the feasibility and superiority of the scheme by comparing it with the traditional packaging scheme and optimizes the scheme according to the experimental results.

The main innovation points of this paper are as follows: (1) A low-power 3D stacked packaging structure based on TSV for AIoT underwater vehicles is proposed. By optimizing the TSV design parameters and vertical interconnection technology, the interconnection length between chips is shortened, the parasitic capacitance and resistance are reduced, and the dynamic power consumption of the chip system is effectively decreased. At the same time, the packaging structure is designed with waterproof and anti-corrosion functions, which can adapt to the harsh underwater environment. (2) An integrated heat dissipation packaging technology combining microchannel heat sinks and PCMs is designed. Aiming at the heat accumulation problem of chips in underwater sealed environments, the microchannel heat sink is used to enhance heat conduction, and the PCM is used to absorb the heat generated by the chip, which improves heat dissipation efficiency while reducing the power consumption of active heat dissipation components. The heat dissipation model of the packaging structure is established, providing a theoretical basis for heat dissipation design. (3) A chiplet-based heterogeneous integration scheme for AIoT underwater vehicle chip systems is proposed. By splitting the chip system into multiple functional chiplets and integrating them into a single package, the functional integration and power consumption distribution are optimized. Different chiplets adopt various low-power design strategies, which realize the balance between high performance and low power consumption, and improve the flexibility and scalability of the chip system.

Transparency:

The authors confirm that the manuscript is an honest, accurate, and transparent account of the study; that no vital features of the study have been omitted; and that any discrepancies from the study as planned have been explained. This study followed all ethical practices during writing.

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